Generating DRC and Electrically Correct Placed-and-Routed Arrays Using the TSMC 7nm Process

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ABSTRACT

The Device Array Flow for 7nm in Virtuoso aims to provide a tight front-to-back loop for circuit designers to verify the performance of their designs in the presence of layout effects. The circuit designer can evaluate the quality of layouts for critical structures to reduce design iterations without performing any layout. The key feature of this flow is the automatic creation of analog device arrays compliant with design rules and electrical constraints. It is based on the Virtuoso Connectivity and Module Generator (ModGen) environments to capture designer intent for placement and routing to create correct by construction layout followed by simulation using the Analog Design Environment (ADE).

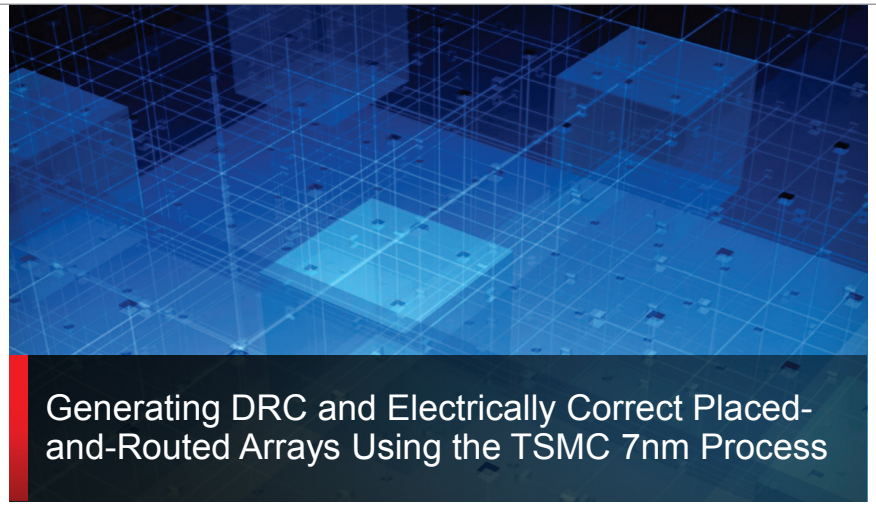
First, the candidate structures are identified and a Device Array generator is applied. The generators can be associated with specific structures or can be generic to allow users to do single row or multi-row layouts. The generators allows users to specify a placement pattern that accounts for m-factored and iterated instances, number of rows, number of columns and dummy devices. In addition, users can specify different guard ring configurations to ensure a high degree of matching.

Secondly, users can specify how the array should be routed. The arrays can be routed using pre-programmed proven routing patterns developed by the TSMC and Cadence IP teams or they can be routed using custom Width Spacing Patterns (WSPs) provided by the customer. A corresponding routing topology will then be created which will not only account for multi-patterning rules, but also Electro-migration (EM) rules. The Electrically Aware Design (EAD) flow uses currents captured using ADE to size the topology based on EM rules. At the end, the router will route the array which will not only be DRC correct, but also electrically correct.

Users can easily save the placement and routing information as presets in order to quickly re-apply to a different set of devices for easy reuse. Engineering Change Orders (ECOs) are also easy - once created, the array can be easily edited by modifying the generator parameters in schematic or layout, and kept in sync between the two through update commands.

Once the generators have been defined, circuit designers can run an analysis of how the physical information impacts the electrical performance. For each generator, the LDE effects can be extracted using PVS or a foundry specific API. The RC parasitics (MEOL and BEOL) can be extracted using the EAD flow. Using ADE, a new netlist is generated that captures the LDE and parasitic effects of each generator and circuit designers can simulate their designs to verify their target specifications. This all happens without requiring the circuit designer to perform any layout operations.

The presentation will showcase real world examples of layouts in 7nm and compare results between schematic simulations, post-layout simulations and simulations done using layouts generated using these generators. The results will demonstrate that allowing users to simulate with early parasitic effects without completing a final layout will result in faster parasitic closure.



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September 2017

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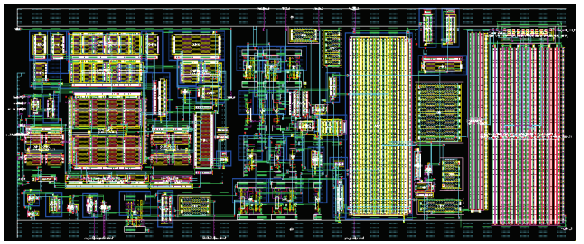
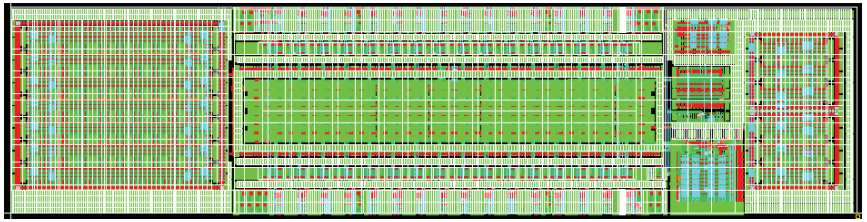
The Way We Design at 7nm Is Very Different than 28nm…





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Problem Statement

- Density plays a key role in the layout for highly matched arrays
  - Uniformity is key to achieving a high level of matching (as seen on previous slide)
  - Abrupt density gradients can have a negative impact on circuit performance
- Pre-layout simulations need to account for physical effe
  - Not only placement and routing, but also density gradient greatly impact simulation results at advanced nodes
- Pre-layout simulations require designers to have acces to *placed* and *routed* layout for critical device structure
  - They require a quick and easy way to get highly matched layout for critical parts of their circuit as part of the design process
- Introduction of highly structured multi-grid row based place and route methodology

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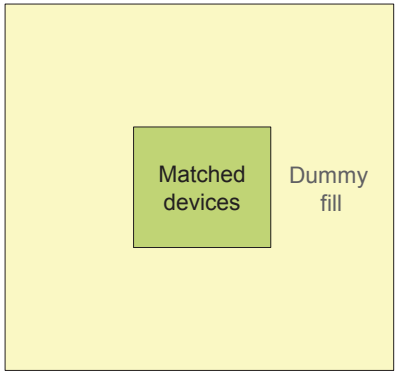
History Behind the Row-Based Methodology

- Cadence IP team has been using the row-based methodology since 28nm
- One of the key drivers of the methodology was poly density gradient effects
  - Matched devices required many microns of dummy poly
  - Could not transition in a short distance from thin gates to thick gates
- The addition of dummy required to negate these effects resulted in a large loss of area



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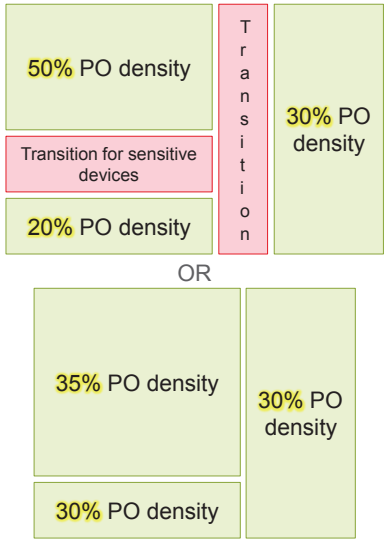
History Behind the Row-Based Methodology



- Two solutions to the problem
  - Waste a lot of area transitioning from different poly density regions
  - Target uniform (+/- margin) poly density in all areas of your layout
- From a layout perspective – if you want to target uniform poly density – what does that look like?
  - Row based and..
  - Everything in the rows looks about the same

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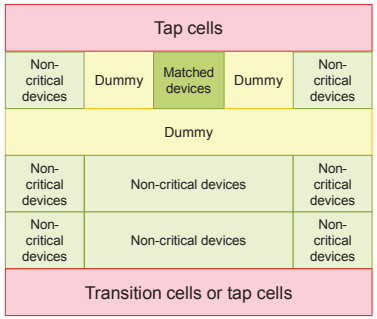
History Behind the Row-Based Methodology

- Advantages are immediately visible for layout
  - Everything looks regular
  - Things started snapping together
  - Complexity of rules abstracted out to a higher level
  - Layout becomes faster
  - Meeting density targets becomes easier
  - And unlike popular belief, does not result in loss of area
- Our IPG team sticks to this methodology for every node since 28nm
  - The engineers swear by it
  - Those who leave, implement methodology at the companies they go to



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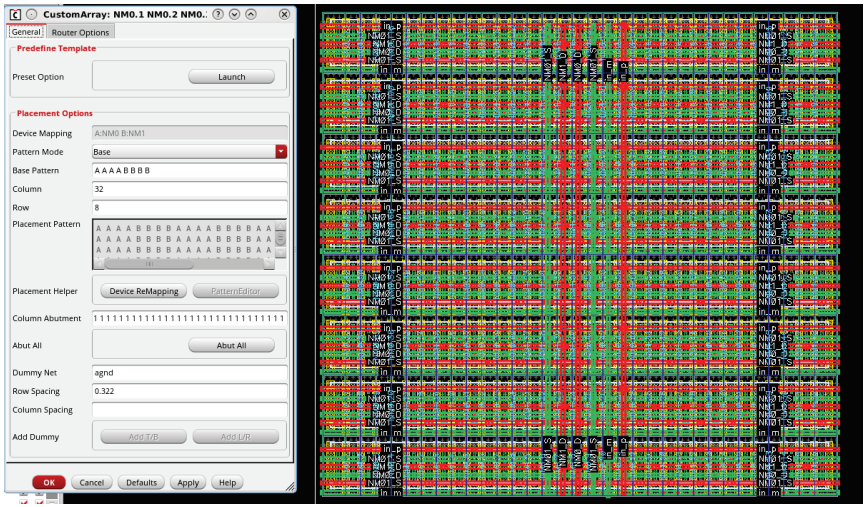
N7 Device Array
Example



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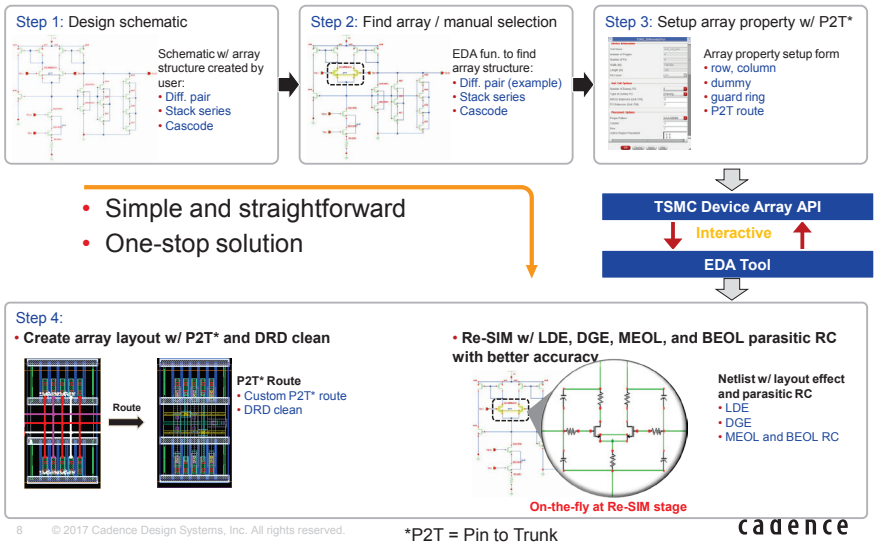
Workflow and Usage Models
Custom device array generation flow



*P2T = Pin to Trunk

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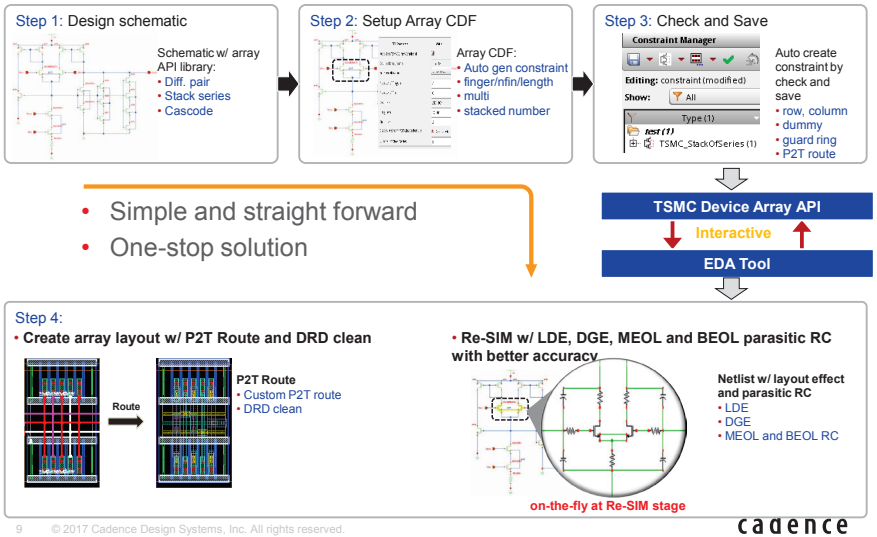
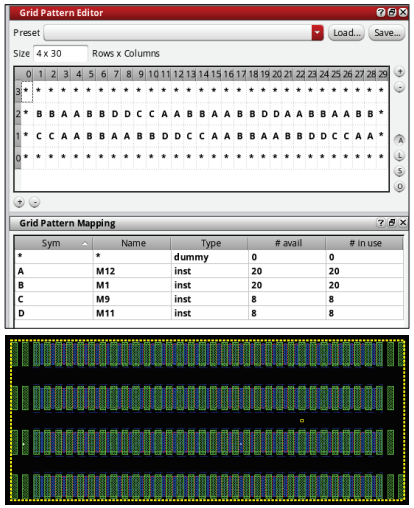
Workflow and Usage Models

Custom device array generation flow



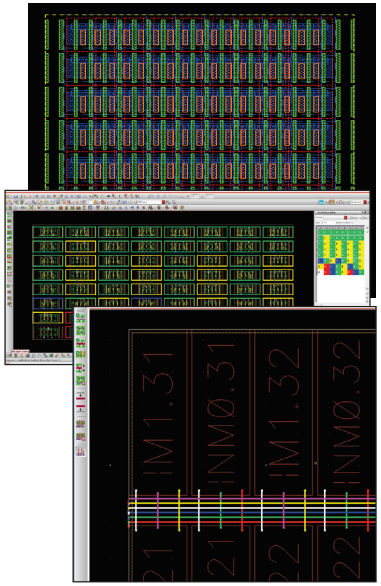
Placement Challenges for Matched Arrays

- Density-gradient effects (DGEs)
- Layout-dependent effects (LDEs)
- Manipulation of a large number of devices in the array
- Sophisticated pattern configurations
- Complex DRC rules
- Precise control over dummies and guard rings
- Dummy backannotation
- Custom, reusable base patterns



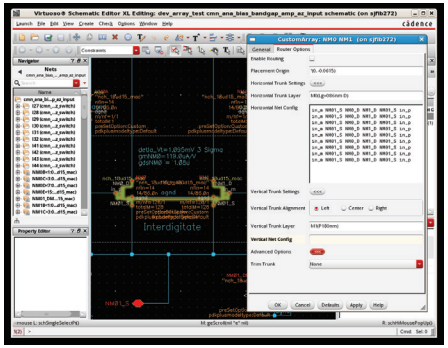
Solution: ModGen-Based Device Arrays

- A newly enhanced module generator (ModGen) infrastructure allows foundries and customers alike to create a template based flow for generating highly matched device arrays
- Using this infrastructure, customers can generate templates for different types of arrays that can create layout while offering users control over
  - # of rows
  - # of columns
  - Dimension of dummy devices
  - Identical guard ring
- These templates act like “super-Pcells” where changing any parameter on the template will cause the array to reconfigure itself and update the layout



Placement Features

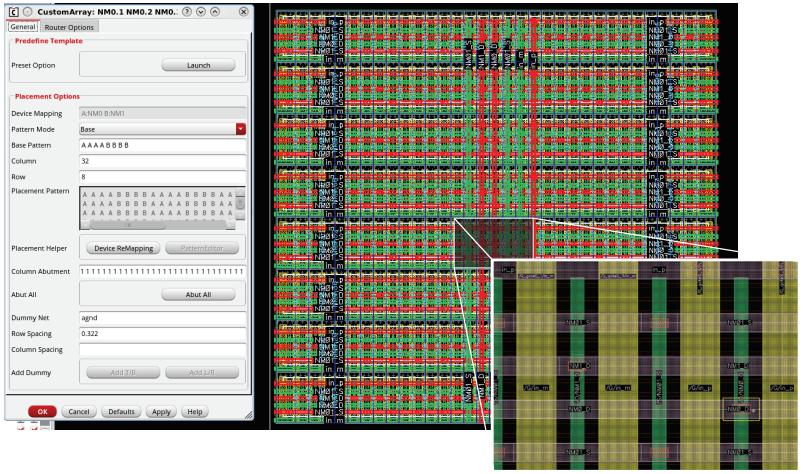
- Introduced in 16FF+ PDK
  - 2014 OIP Conference: Managing 16nm IC Design Challenges for Custom and Analog Designers
  - Version: T-N16-CR-SP-006-W1, V1.0_2p2a and above
- Now certified at 10 and 7nm
- Example generators
  - Differential pairs
  - Cascodes
  - Stack of series devices
  - HiR resistors
- Many customers building their own customized generators
  - Similar to PCells with more opportunity to differentiate



Supported structures

N7 Differential-Pair Generator Example

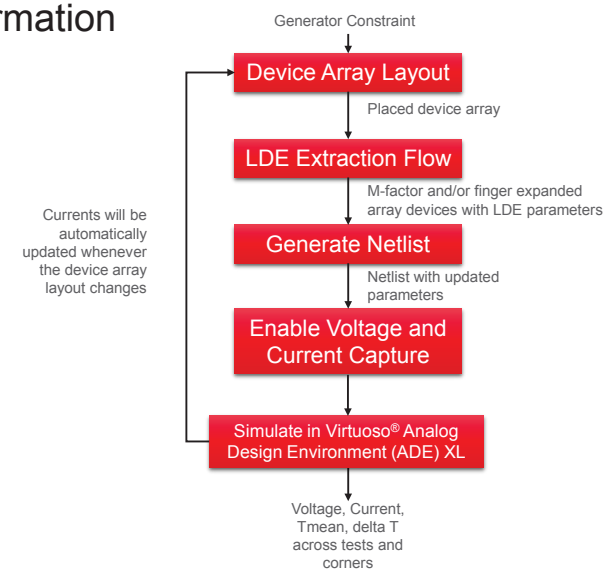
Layout and parameter editing



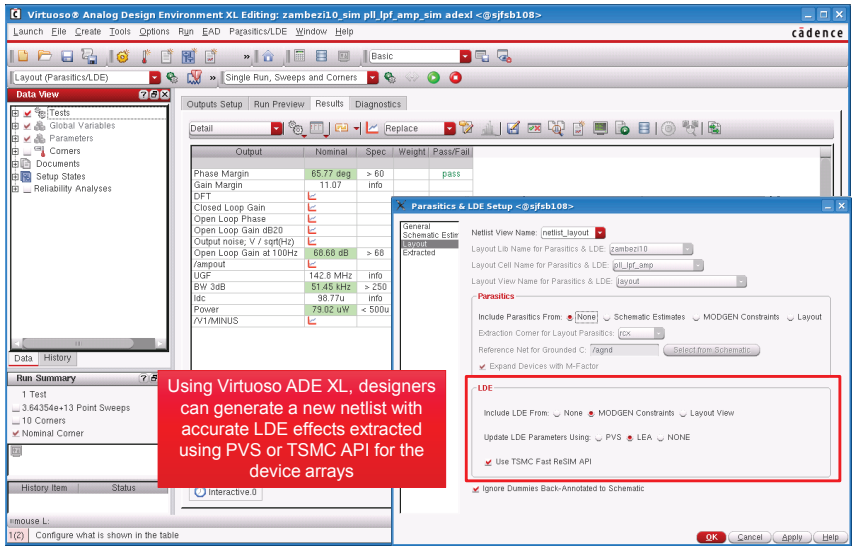
N7 routing

Simulate and Capture Currents with Placed Array

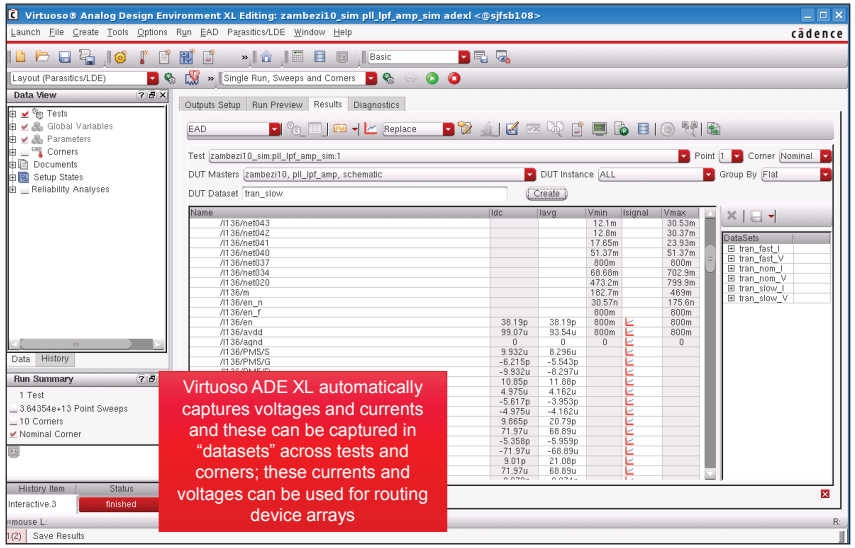
Simulation Flow with LDE to Capture Electrical Information



LDE Extraction Flow

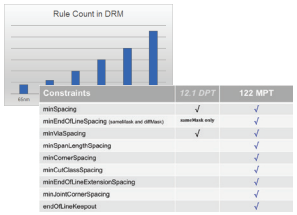


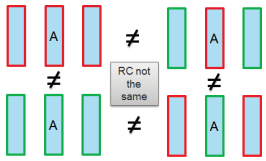
Capture Voltages and Currents

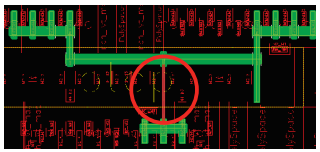


N7+ Routing Challenges

- Basic design rule complexity
- Electromigration (EM) complexity as tiny wires driving a ton of current
- Routing parasitic C are in the same order of magnitude as intrinsic capacitances (gate, etc.)
  - Early layout estimates required to confirm circuit architectures
  - Manual capture of the parasitic capacitance on schematics is challenging and generally inaccurate
- Routing resistance has large impact on performance for high-frequency circuits
  - Early layout extractions with representative floorplan required to confirm circuit architecture
  - Manual estimates of the routing resistance can be inaccurate due to the number of layers contributing to the overall resistance, including lower-level metals



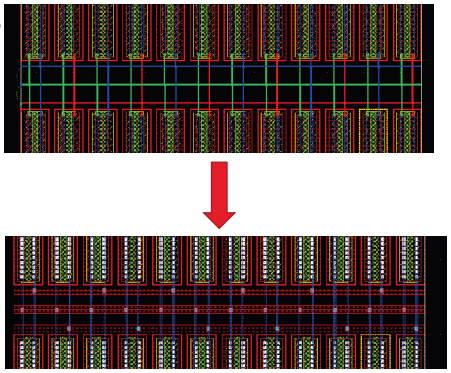




EM Violation

Solution: Topology-Based P2T Routing

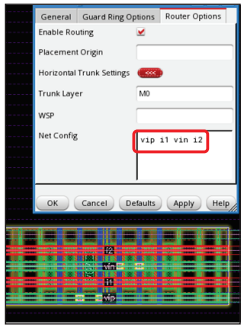
- Topology captures user intent for routing without any physical shapes
  - Locations of routes in a channel or over a device in tandem with width spacing patterns (WSPs)
  - Spacing within the channel
  - Order of routes
  - Color and width of routes
  - Via types
- Topology is automatically updated to reflect changes in width due to currents or self heating
- Once the topology is defined, the P2T can be invoked to route the array based on the specification of the topology

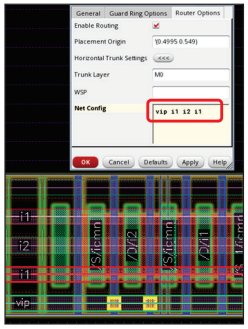


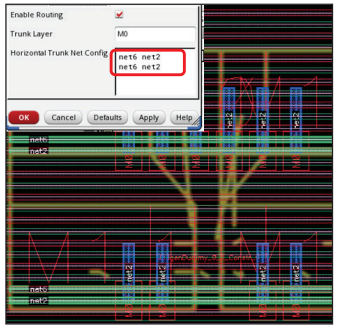
N7+ Routing of Device Arrays

WSP support

- Specify net order on Router Options form to route on top of WSPs
- Net order can be specified for each row of the array
  - Defaults are provided

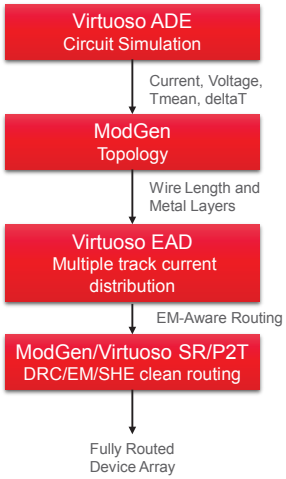


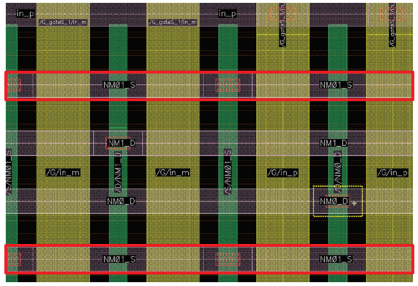




Using Virtuoso Layout Suite EAD

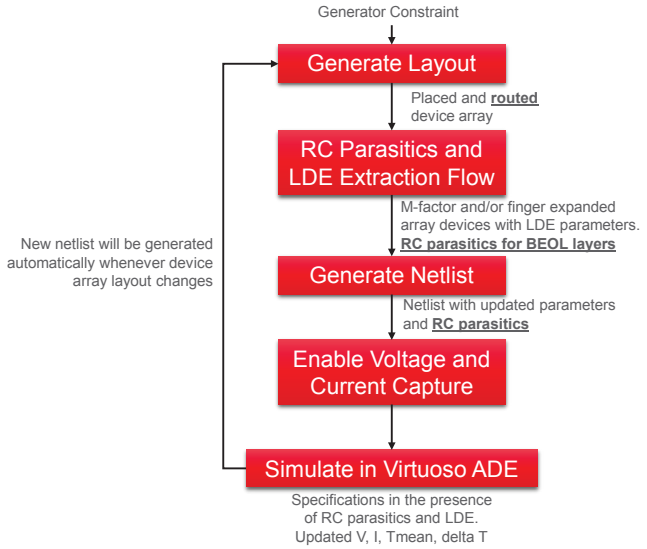
Topology and Virtuoso Space-Based Router/P2T Router on 7nm Arrays



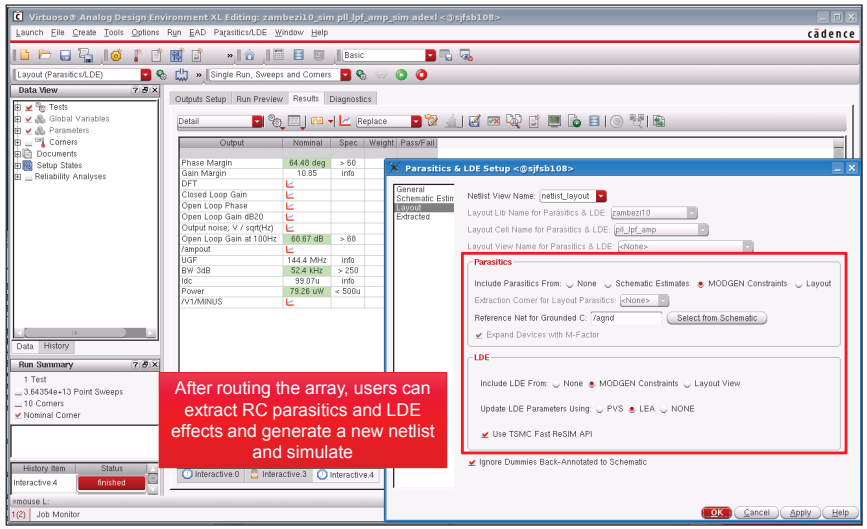


N7 WSP routing (EM aware)
Multiple track distribution

Re-Simulation Flow with RC Parasitics and LDE



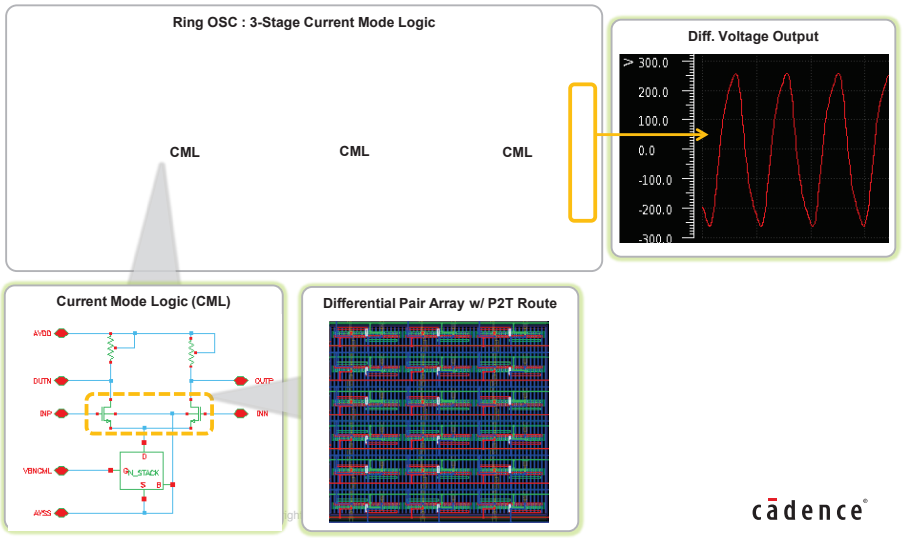
Re-Simulating with RC Parasitics and LDE



Real-World 7nm Examples and Solutions

- Cadence IP Factory
- TSMC
- Collaboration between leading semiconductor, foundry, and EDA companies is key

Example 1
Ring OSC: 3-stage CML (N10)



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Example 1 (cont)
Ring OSC: 3-stage CML

- Accuracy comparison
  - Pre-SIM – Simulating with schematic
    - Turn on pre_simu model flag : MEOL RC
  - Re-SIM - **Simulating with Arrays**
    - Extract Differential Pair Device Array : LDE, MEOL RC, BEOL C only
  - Post-SIM – Simulating full GDS Layout
    - Extract entire CML GDS layout
- Design stimulus and results
  - Simulator: spectre
  - Transient time: 10ns

Item	Pre-SIM	Re-SIM	Post-SIM
Output Cycle Time	94.912ps	164.222ps	221.483ps
Output Frequency	10.536GHz	6.0893GHz	4.515GHz

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Example 2
Band gap - differential input (proprietary circuit / N7+)

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- Device array simulation (Re-SIM) vs. post-layout simulation (Post-SIM)

Output	Test	Min Diff	Min %	Max Diff	Max %
BG_Gain	bandgap_dc_stb_ac	3.92p	1.558e-10	7.28p	2.894e-10
Bandwidth	bandgap_dc_stb_ac	2.326K	0.122	53.55K	0.6643
DC Gain	bandgap_dc_stb_ac	475.3u	0.0005339	4.086m	0.008101
Gain Margin	bandgap_dc_stb_ac	104.9m	0.6607	1.322	5.302
Offset	bandgap_dc_stb_ac	113.1n	0.09698	182.1n	0.1337
PSRR_100	bandgap_dc_stb_ac	69.34u	0.0003786	349.1m	0.3868

- Schematic simulation (Pre-SIM) vs. Post-layout simulation SIM)(Post-SIM)

Output	Test	Min Diff	Min %	Max Diff	Max %
BG_Gain	bandgap_dc_stb_ac	30.2f	1.201e-12	6.92p	2.751e-10
Bandwidth	bandgap_dc_stb_ac	3.317	9.189e-05	36.09K	0.5791
DC Gain	bandgap_dc_stb_ac	16.66u	2.277e-05	4.75m	0.008244
Gain Margin	bandgap_dc_stb_ac	1.636	7.66	4.332	17.88
Offset	bandgap_dc_stb_ac	11.77p	2.935e-05	157.1n	1.42
PSRR_100	bandgap_dc_stb_ac	71.58u	0.0003897	347.1m	0.383

- Gain margin measured as off by >17% without device array across 180 corners

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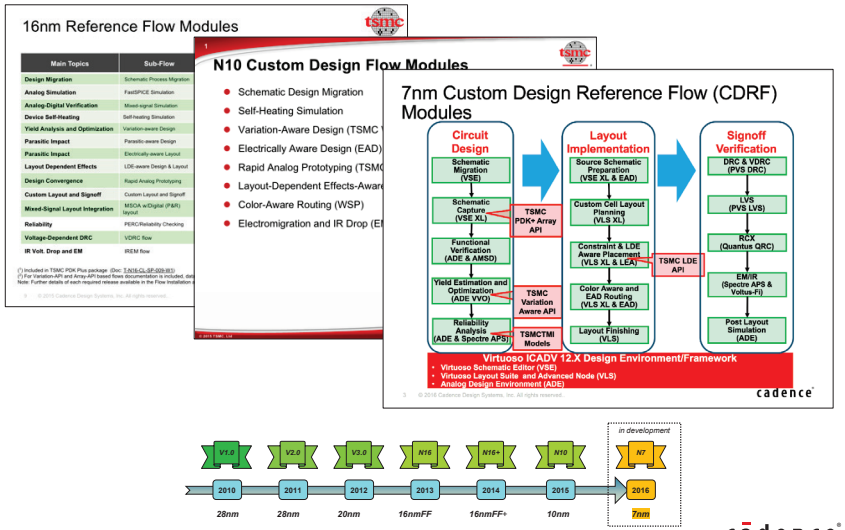
For More Detailed Information

Robust reference flows



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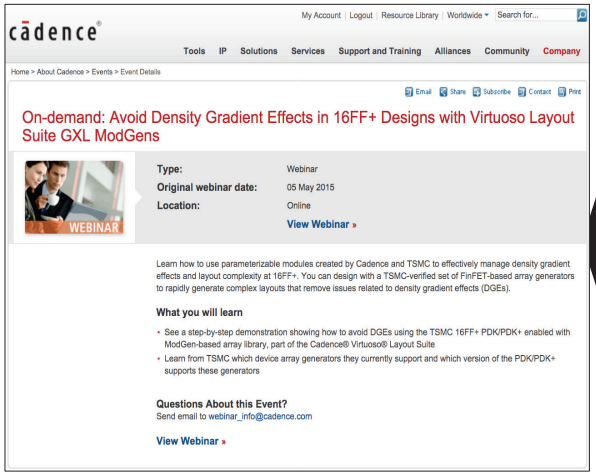
For More Detailed Information – Recorded webinars

Innovative solutions with proven results



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- Cadence Taiwan
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